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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/956,973	09/21/2001	Yasurou Matsuzaki	10035-00079	5655

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EXAMINER
TRAN, LONG K

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/956,973	MATSUZAKI ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *1-12,16-25 and 29-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-15 and 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

El ction/Restrictions

1. Applicant's election without traverse of claims **13 – 15** and **26 – 28** in Paper No. **5** is acknowledged.

2. Claims **1 – 12, 16 – 25** and **29 – 41** withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claim, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. **5**.

3. Claims **13 – 15** and **26 – 28** are presented for examination.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on September 21, 2001.

Information Disclosure Statement

5. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on September 21, 2001.

Information disclosed and lists on PTO 1449 were considered.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims **13 – 15** are rejected under 35 U.S.C. 102(e) as being anticipated by Suyama (US Patent No. 6,403,463).

Regarding claim **13**, figures 1 – 3 illustrate a multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, one of the first and second chips comprising: a first wiring layer 56 provided on a semiconductor substrate 1; a second wiring layer 57 provided on an insulating layer covering 52, the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips; a plurality of first electrodes (having terminals 2a) provided in the first wiring layer, and a second electrode provided on each of the conductive lines, each conductive line being configured to interconnect the plurality of first electrodes and the second electrode.

Regarding claim **14**, figures 1 – 3 illustrate a multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, one of the first and second chips comprising: a first wiring layer 56 provided on a semiconductor substrate 1; a second wiring layer 57 provided on an insulating layer covering 52, the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips; a first electrodes provided in the first wiring layer, and a plurality of second electrodes (having terminals 2a) provided on each of the conductive lines, the conductive lines being configured to interconnect the first electrode and the plurality of second electrodes.

Regarding claim **15**, figures 1 – 3 illustrate a multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, one of the first and second chips comprising: a first wiring layer 56 provided on a semiconductor substrate 1; a second wiring layer 57 provided on an insulating layer covering 52, the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips; a plurality of first electrodes (having terminals 2a) provided in the first wiring layer, and a plurality of second electrodes (having terminal 2a) provided on each of the conductive lines, the conductive lines being configured to interconnect the plurality of first electrodes and the plurality of second electrodes.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **26 – 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suyama (US Patent No. 6,403,463) in view of King et al. (US Patent No. 6,429,528).

Regarding claims **26 – 28**, Suyama discloses the claimed invention of claim 13 except for the conductive lines forming a large-size bus; the conductive lines forming a bus that interconnects the circuit components of the semiconductor apparatus; and one of the first and second chips includes external connection electrodes, the external

connection electrodes being disposed in peripheral portions of said one of the first and second chips which do not interfere with the other of the first and second chips.

King et al. disclose conductive bus 32 (figs. 1, 3 and 4) that interconnects individual lead of the circuit components of the semiconductor apparatus (col. 5, lines 33 – 56; col. 6, lines 42 – 61); common electrode suitable for electrically providing the signal to another, external circuit, such as a PWB.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the conductive lines forming a large-size bus; the conductive lines forming a bus that interconnects the circuit components of the semiconductor apparatus; and one of the first and second chips includes external connection electrodes, the external connection electrodes being disposed in peripheral portions of said one of the first and second chips which do not interfere with the other of the first and second chips as taught by King et al. into Suyama's apparatus in order to eliminate high wiring density in the apparatus and to provide for redundant back-up in the event of bad chip or signal line deteriorated.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Okamura (US Patent 5,619,472) and Ahn et al. (US Patent No. 6,441,479) disclose a system-on-a-chip with multi-layered metallized through-hole and semiconductor memory device similar to Suyama (US Patent No. 6,403,463) and King et al. (US Patent No. 6,429,528).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 703-305-5482. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7466 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Long Tran

April 11, 2003

HOAI HO
PRIMARY EXAMINER